

Solder Joint Health Monitoring Testbed

Mike Delaney, James Flynn, Mark Browder

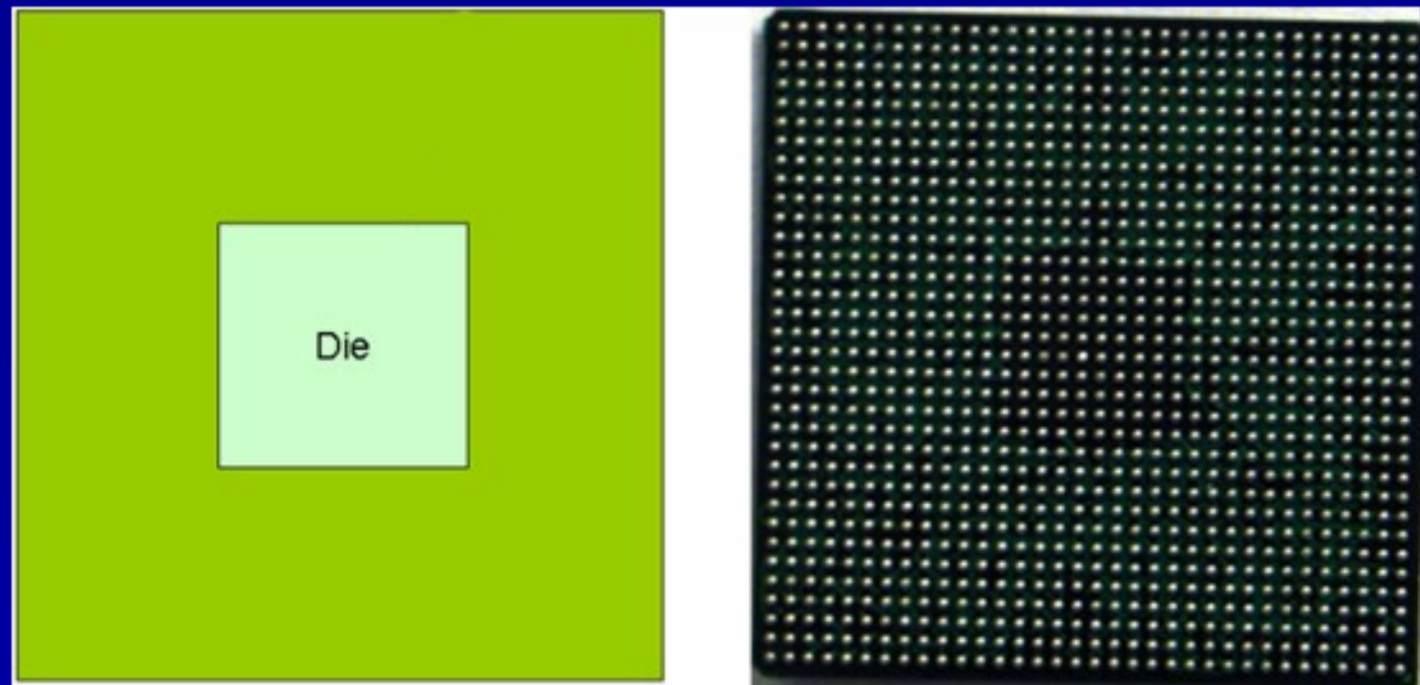
Flight Instrumentation Branch, NASA Dryden Flight Research Center, Edwards CA

Michael.M.Delaney@nasa.gov

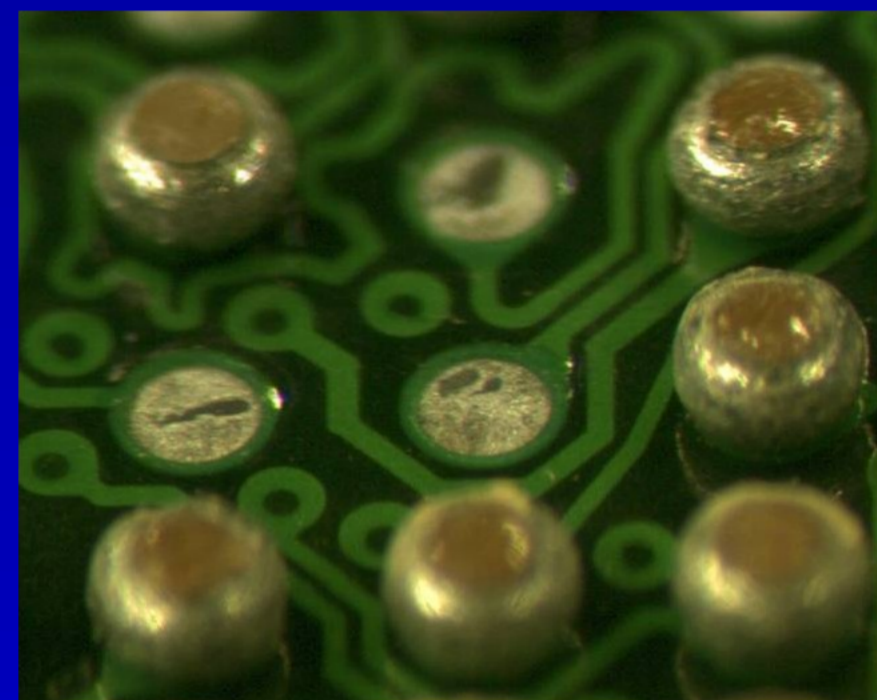
Motivation

Ball Grid Array (BGA) chip packages are a relatively new technology that allows for increased pin density and better signal integrity than other package types. BGA packages are the only option available for many newer and high performance FPGAs. BGA packages use solder balls extending from the bottom of the chip package instead of leads extending from the sides of a package. The solder joints can only be inspected using X-Ray or some specialized optical systems.

These solder joints can fail under environmental stress from temperature cycling, shock and vibration. Typically the failure mode is an intermittent fault, rather than a full failure, and is likely to appear functional when it is not under stress. An effective method of monitoring solder joint health in real time will detect failures before the unit has an operational fault. This enables a higher confidence the use of BGA packages in high reliability systems.



Chip Die and BGA package, courtesy and permission of Ridgetop Group



Damaged and healthy solder joints, courtesy and permission of Ridgetop Group

Research Program Overview

A method of monitoring the health of selected solder joints, called SJ-BIST, has been developed by Ridgetop Group Inc. under a Small Business Innovative Research (SBIR) contract.

The primary goal of this research program is to test and validate this method in a flight environment using realistically seeded faults in selected solder joints. An additional objective is to gather environmental data for future development of physics-based and data-driven prognostics algorithms.

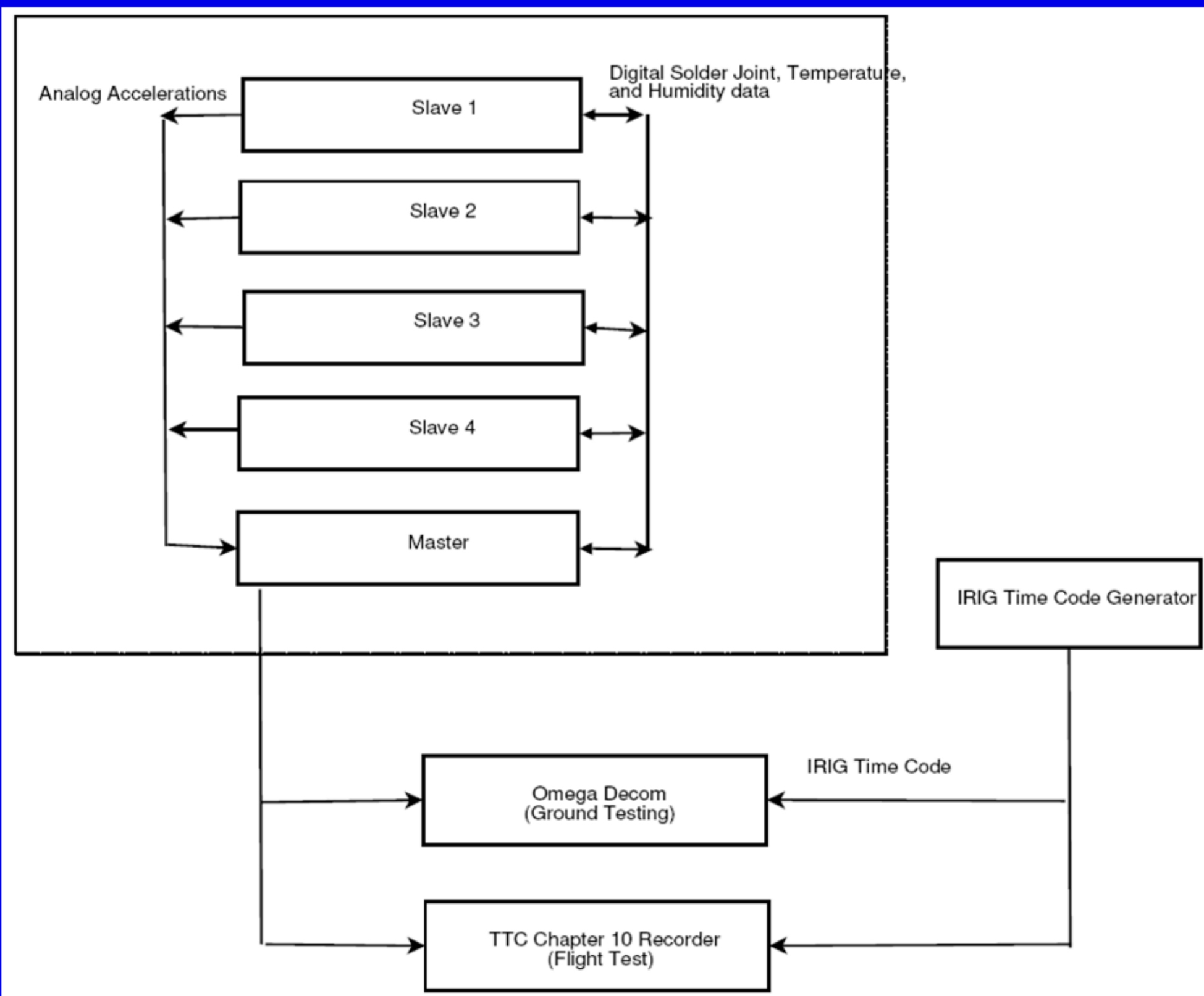
A test board is being designed using a Xilinx FPGA. These boards will be tested both in flight and on the ground using a shaker table and an altitude chamber.

System Description and Block Diagram

The system was designed to be easily integrated into research aircraft and to use existing instrumentation infrastructure, such as time and data recording. Each system consists of five test circuit boards, and generates one output stream. The output is formatted as Inter-Range Instrumentation Group (IRIG) 106 compatible Pulse Code Modulation (PCM). IRIG is a standard used by NASA Dryden for research aircraft instrumentation systems. The master and slave circuit boards use the same design, the FPGA bitstream is the only difference between the master and slave circuit boards.

The system is set up to determine solder joint health on select FPGA pins, and also to collect temperature, pressure, humidity and analog acceleration from each board. All acceleration data will be digitized at 50 kHz on the master board; this simplifies signal timing and synchronization for the design. All of the other sensor data is digitized on the slave boards, and is sent via HDLC to the master board. The master board collects all of the data and generates the output stream.

For ground testing, the PCM output will be monitored using an Omega 3000 PCM telemetry processing system. In flight, the data will be recorded using a Teletronics Technology Corporation (TTC) IRIG Chapter 10 compliant data recorder.



System Block Diagram

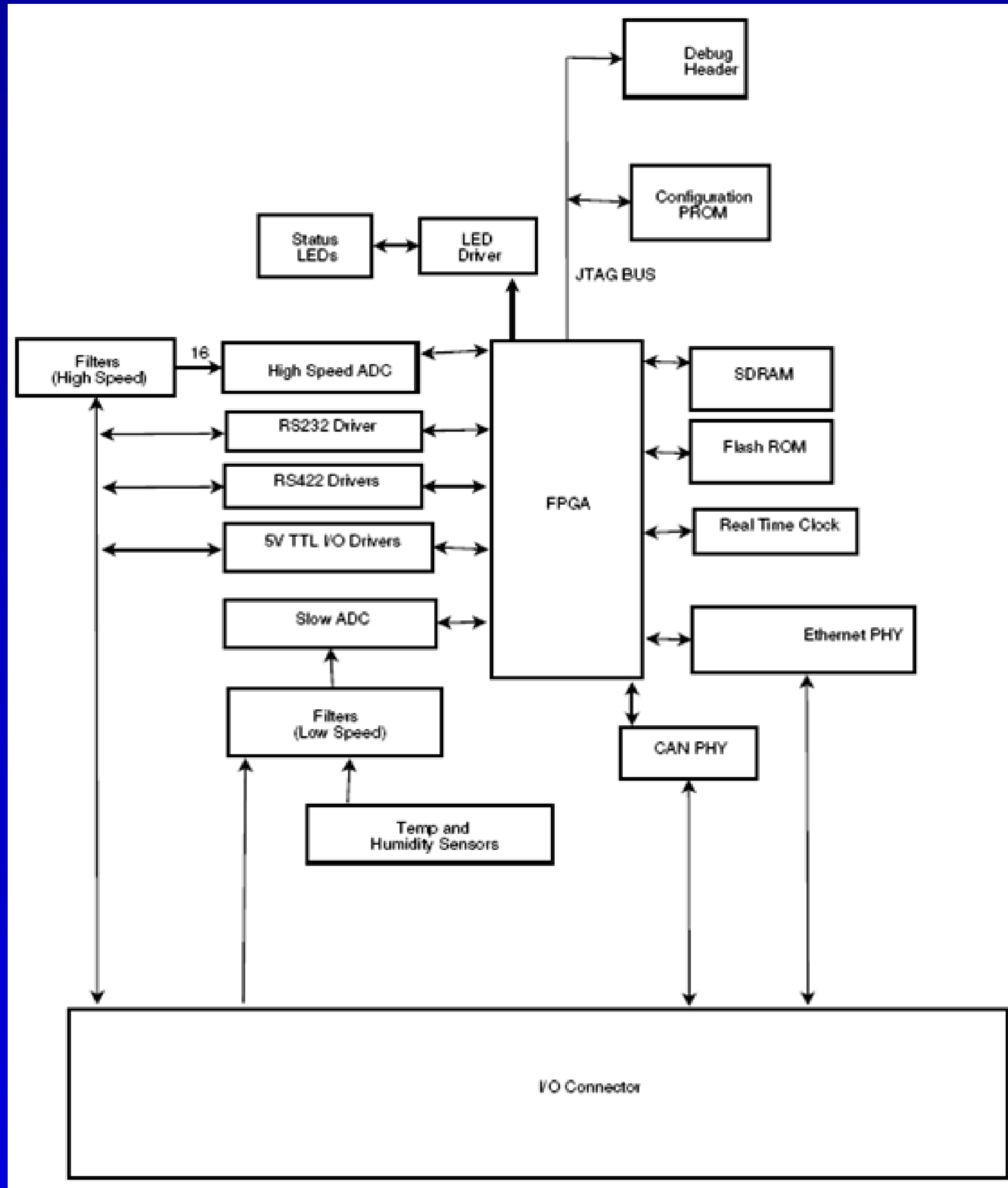
Circuit Board Description and Block Diagram

The circuit will be constructed on a multi-layer circuit board designed to fit a standard 3"X6" footprint used at NASA Dryden. The master and slave boards will be identical in construction; the only difference will be the FPGA bitstream. A Spartan 3A DSP FPGA in a 676 pin BGA package will be located close to the center of the board where the most stress is expected to occur. The FPGA will detect solder joint failures as well as handling all the I/O for sensors and data output.

Digital temperature, humidity, and pressure sensors will be located on the board. The board will have 8 ADC channels sampled at 1kHz and 16 ADC channels sampled at 50kHz. The 1kHz ADC channels will be for future expansion of the system and the 50 kHz ADC channels will be used by the master board to digitize the output of accelerometers placed on each slave board.

The board will have 256MB of SDRAM and 32MB of Flash memory. The onboard memory will allow the use of a MicroBlaze soft-core CPU which will be used to send data frames over Ethernet for testing. CAN, RS-232, and RS-422 physical layers will be included on the board to allow general purpose I/O for future expansion.

The board will run on 28VDC power which is stepped down to 5V through a DC-DC converter. The 5V power will be provided to separate voltage regulators to produce the voltage levels required by FPGA and other circuitry. The voltage levels required on the board are 5V, 3.3V, 1.8V, and 1.2V.

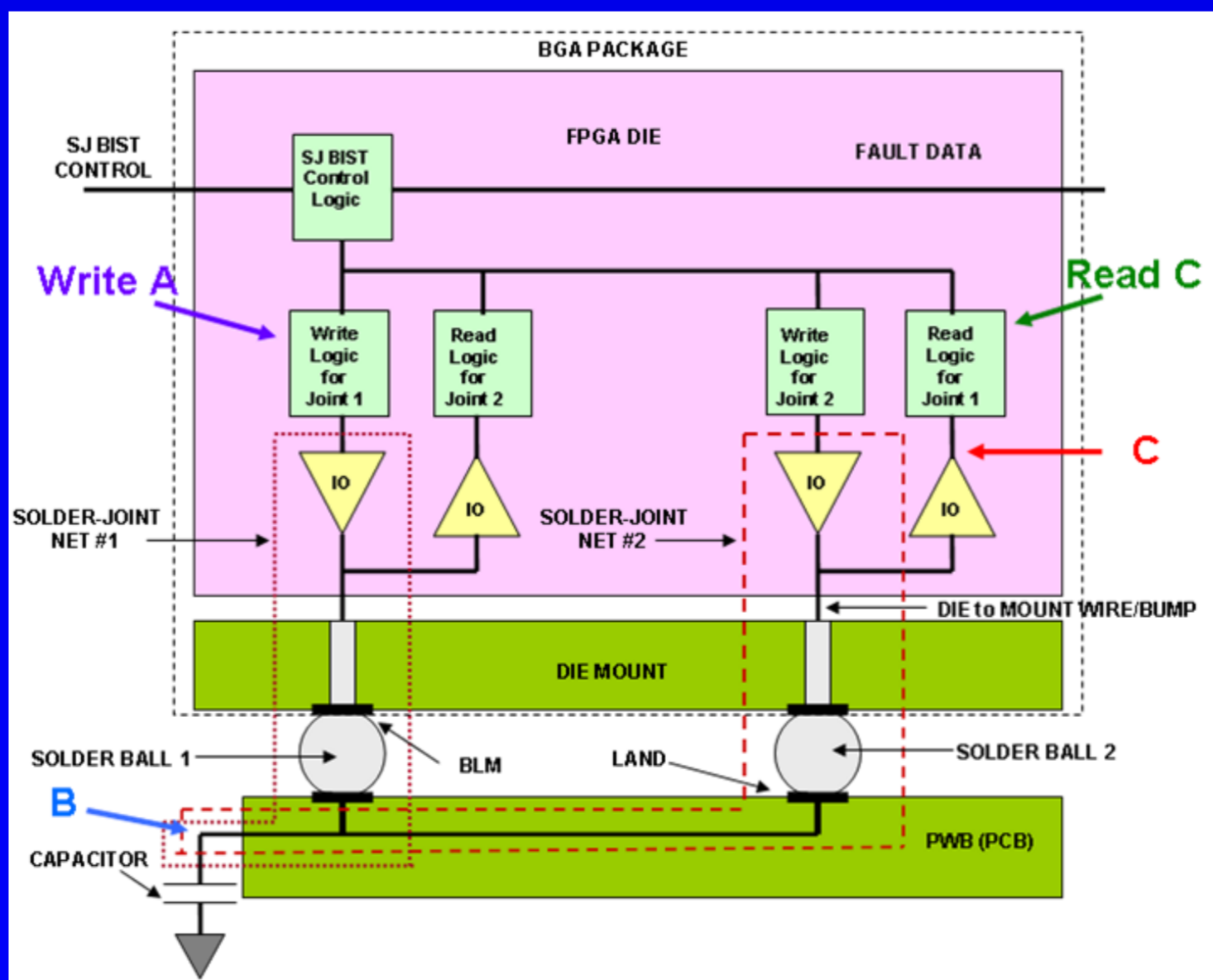


Circuit Board Block Diagram

Solder Joint Failure Detection

The solder joint failure detection method, SJ-BIST, requires two dedicated FPGA I/O pins for each solder joint monitored. The two pins are connected to each other, and to a capacitor, as shown in the schematic below. Alternating reads and writes are done on each pin, and the change in resistance of a fractured or cracked solder joint will change the time constant of the circuit.

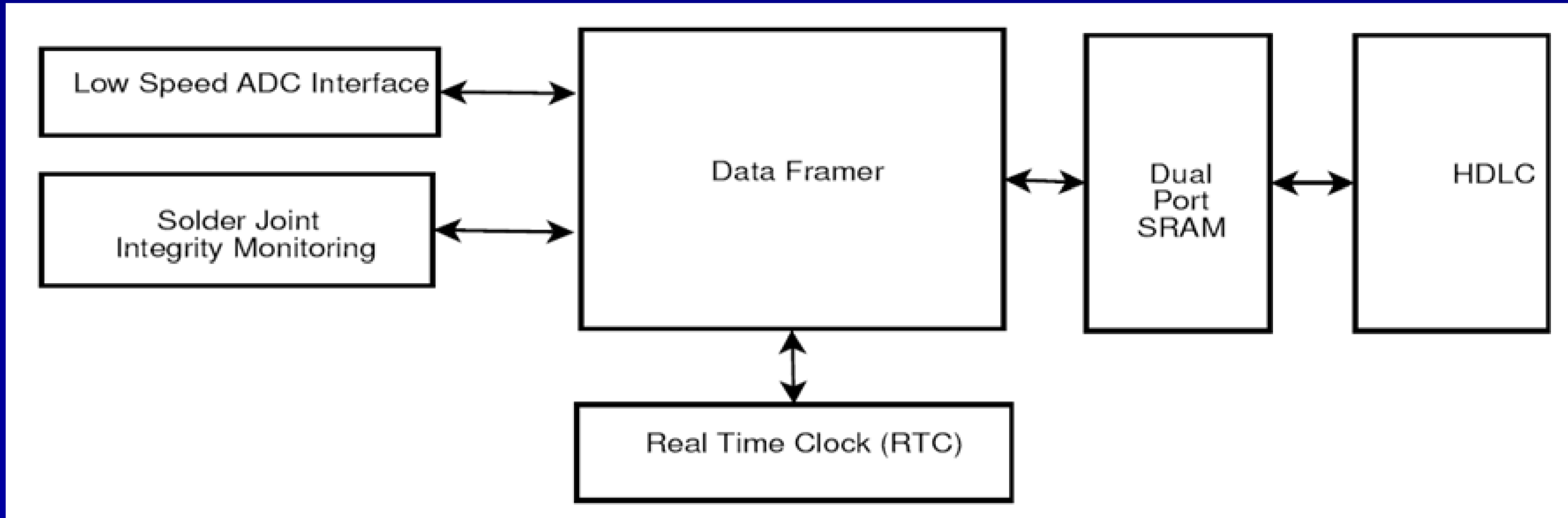
The solder balls on the corners of the package, and near the corners of the die within the package are usually the joints that break first. A small number of test pins should provide warning of solder ball failure while the chip is still functional.



SJ-BIST Block Diagram, courtesy and permission of Ridgetop Group

Slave FPGA Description

The slave FPGA design is responsible for monitoring its own solder joint health, and collecting low-speed data including pressure, temperature, and humidity. This data is time-tagged and then sent to the system's master FPGA over High-Level Data Link Control (HDLC). The majority of FPGA resources are not currently used and are available for future expansion.

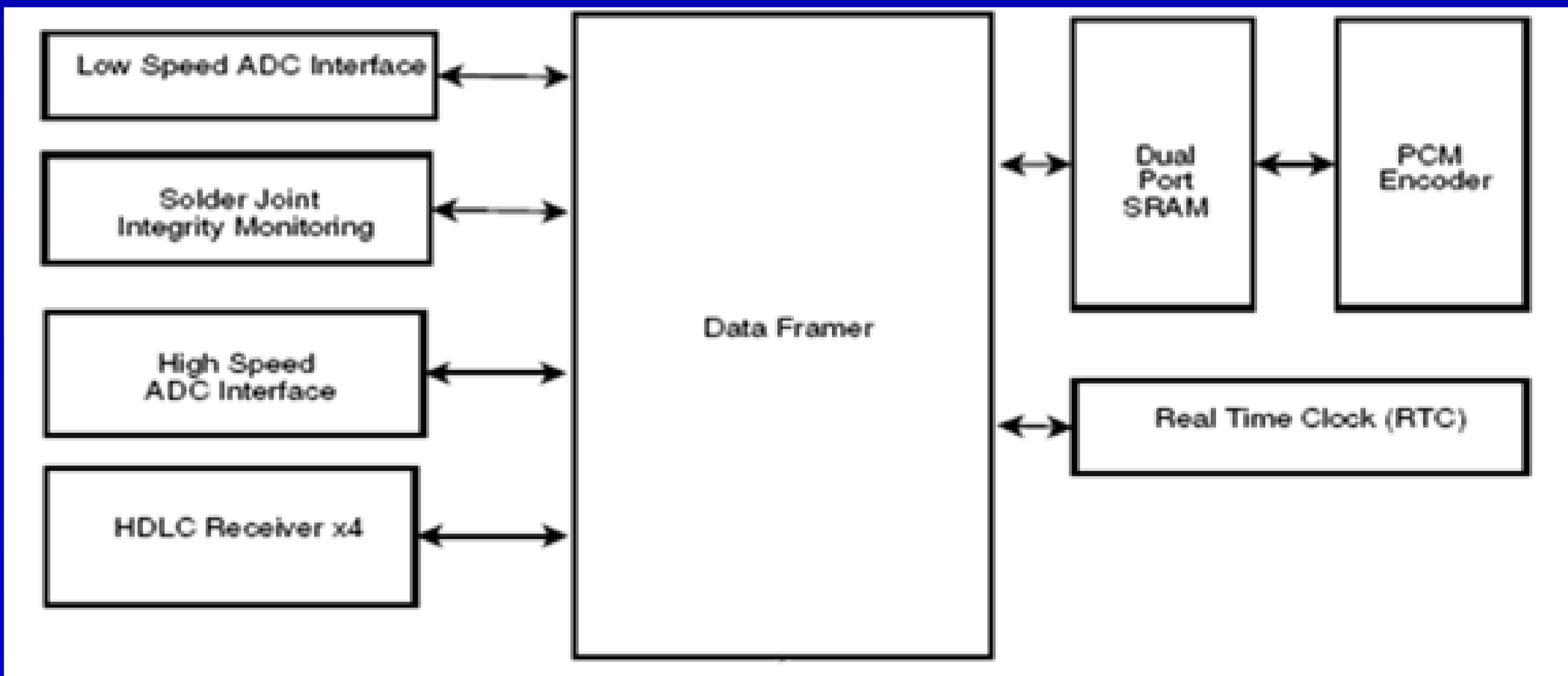


Slave FPGA Block Diagram

Master FPGA Description

The master FPGA has multiple functions. It receives data from the other four boards in the system, digitizes the accelerometer signals from all of the system boards, and collects data on its own solder joint health and board environmental data.

The data is formatted as an IRIG 106 compliant PCM stream. The master FPGA has sufficient resources available to implement a soft-core RISC CPU to run prognosis algorithms once they are developed.



Master FPGA Block Diagram

Test Plan

Testing will be conducted in two phases. The first phase is to conduct testing in an altitude/temperature chamber and on a shaker table. This testing will be representative of environmental conditions encountered in an unpressurized avionics bay on high performance research aircraft.

The second phase of testing will consist of flight testing on one of NASA Dryden's F-18 research aircraft, shown below. The F-18 is instrumented to collect and record data from the avionics bus, including inertial data, and has a Differential Global Position System (DGPS) system. Two systems, for a total of ten test boards, will be installed in avionics bays. One of the avionics bays dedicated to the research instrumentation system is shown below.



F-18/852 Avionics Bay with research instrumentation system

Future Work

Future research items are still in the formulation stage. Ideas include investigating if this technology will work with Column Grid Array (CGA) packages as well, which are similar to BGA and are very common in space flight, and development of prognostics algorithms to calculate the remaining useful life of solder joints based upon environmental loading.

Acknowledgements

The SJ-BIST technology was supported under the Department of Defense SBIR Program at the Naval Air Systems Command, Joint Strike Fighter Program. The NASA Aviation Safety Program conducted accelerated printed circuit board life-cycle evaluation under a partnership developed by the NASA Dryden Innovative Partnerships Office.